

FIG. 1

External address (A0, bA0)

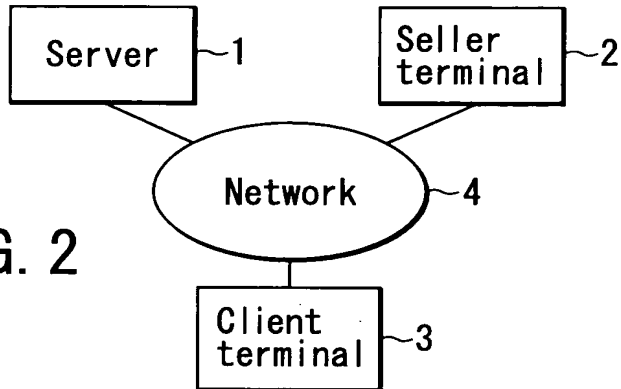


FIG. 2

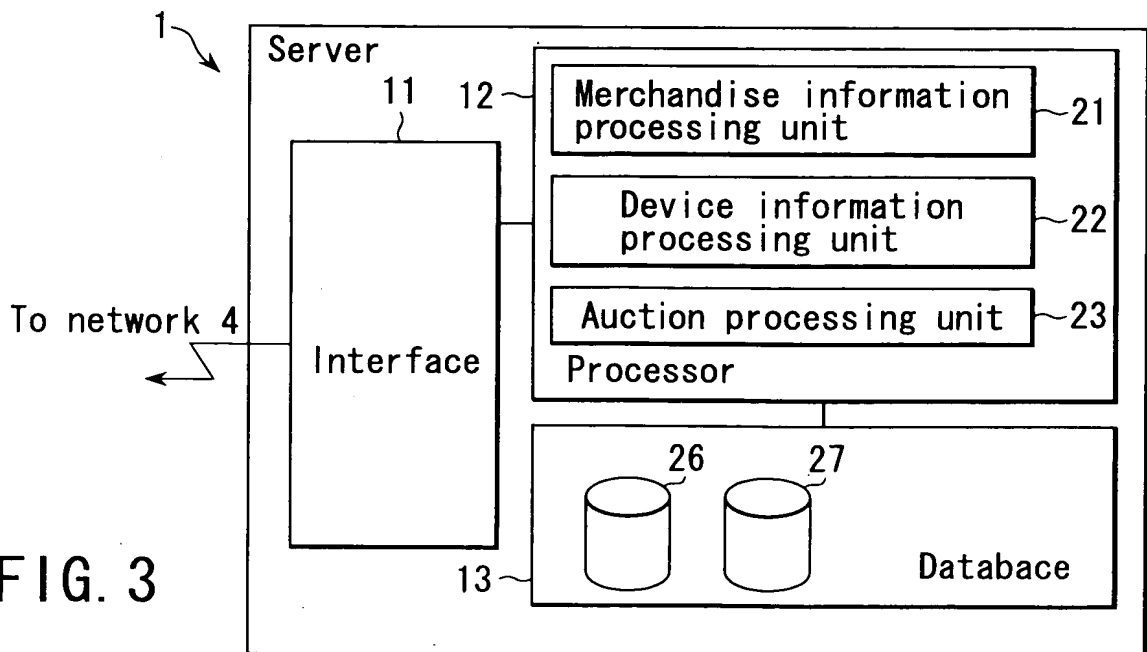


FIG. 3

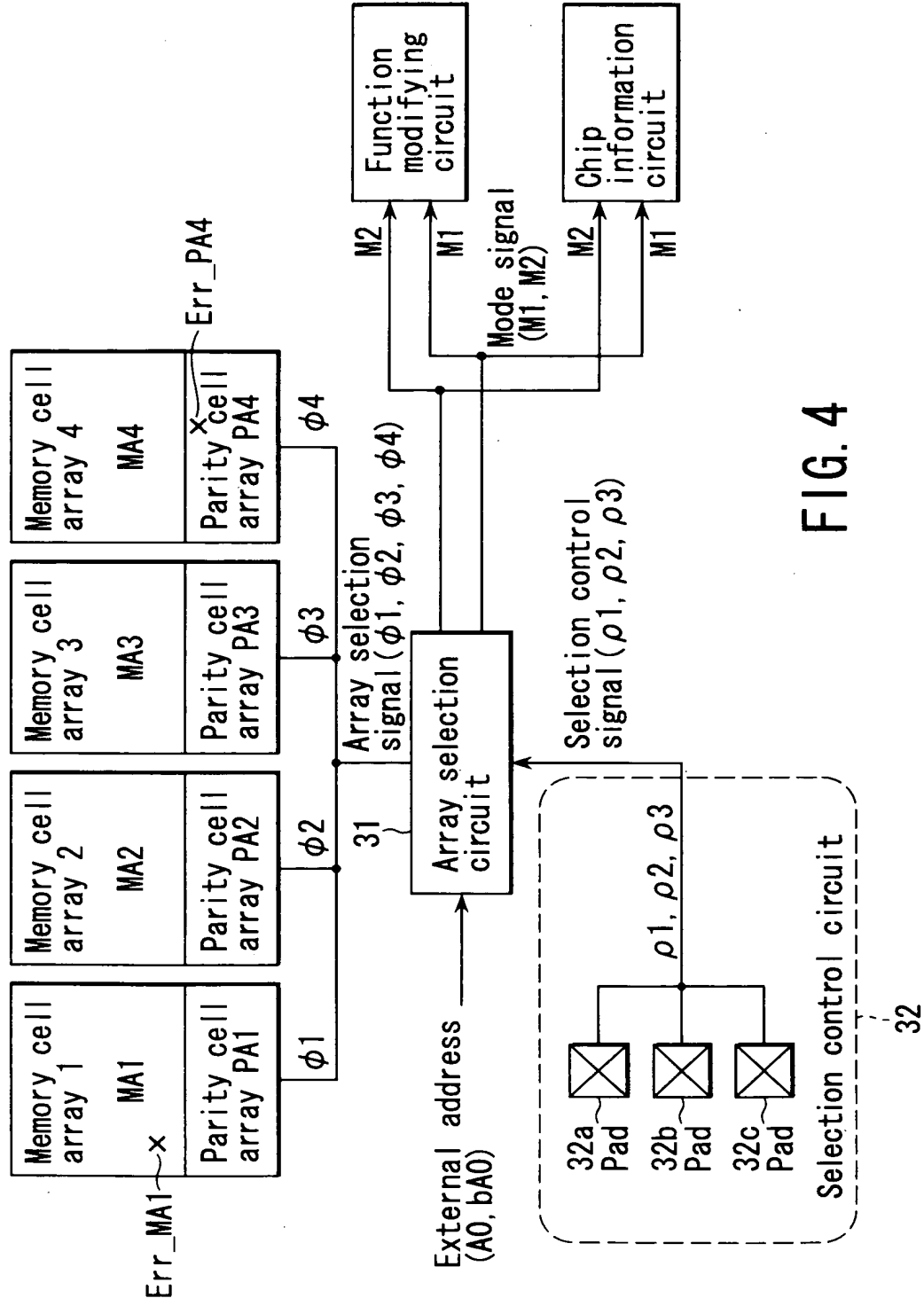


FIG. 4

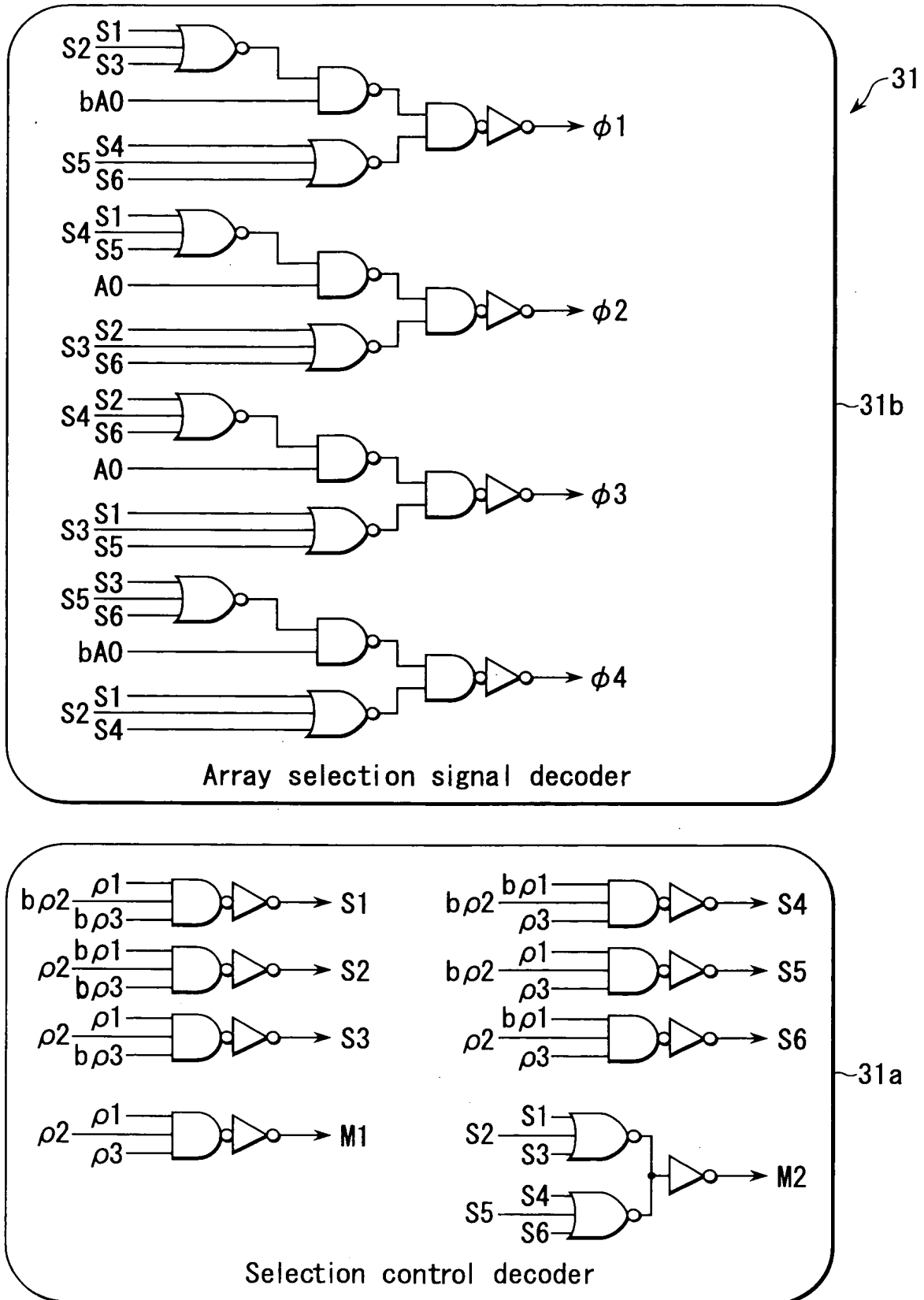


FIG. 5

	Selected array	$\phi 1$	$\phi 2$	$\phi 3$	$\phi 4$	$\rho 1$	$\rho 2$	$\rho 3$	A0	M1	M2
1	MA1 & MA2	1	1	0	0	1	0	0	-	0	1
2	MA1 & MA3	1	0	1	0	0	1	0	-	0	1
3	MA1 & MA4	1	0	0	1	1	1	0	-	0	1
4	MA2 & MA3	0	1	1	0	0	0	1	-	0	1
5	MA2 & MA4	0	1	0	1	1	0	1	-	0	1
6	MA3 & MA4	0	0	1	1	0	1	1	-	0	1
7	MA1 & MA4	1	0	0	1	0	0	0	1	0	0
8	MA1 & MA2	1	0	0	1	1	1	1	1	1	1
9	MA2 & MA3	0	1	1	0	0	0	0	0	0	0
10	MA2 & MA3	0	1	1	0	1	1	1	0	1	1

Default:
A0 = "1" Array MA1 & MA4 are selected
A0 = "0" Array MA2 & MA3 are selected

FIG. 6

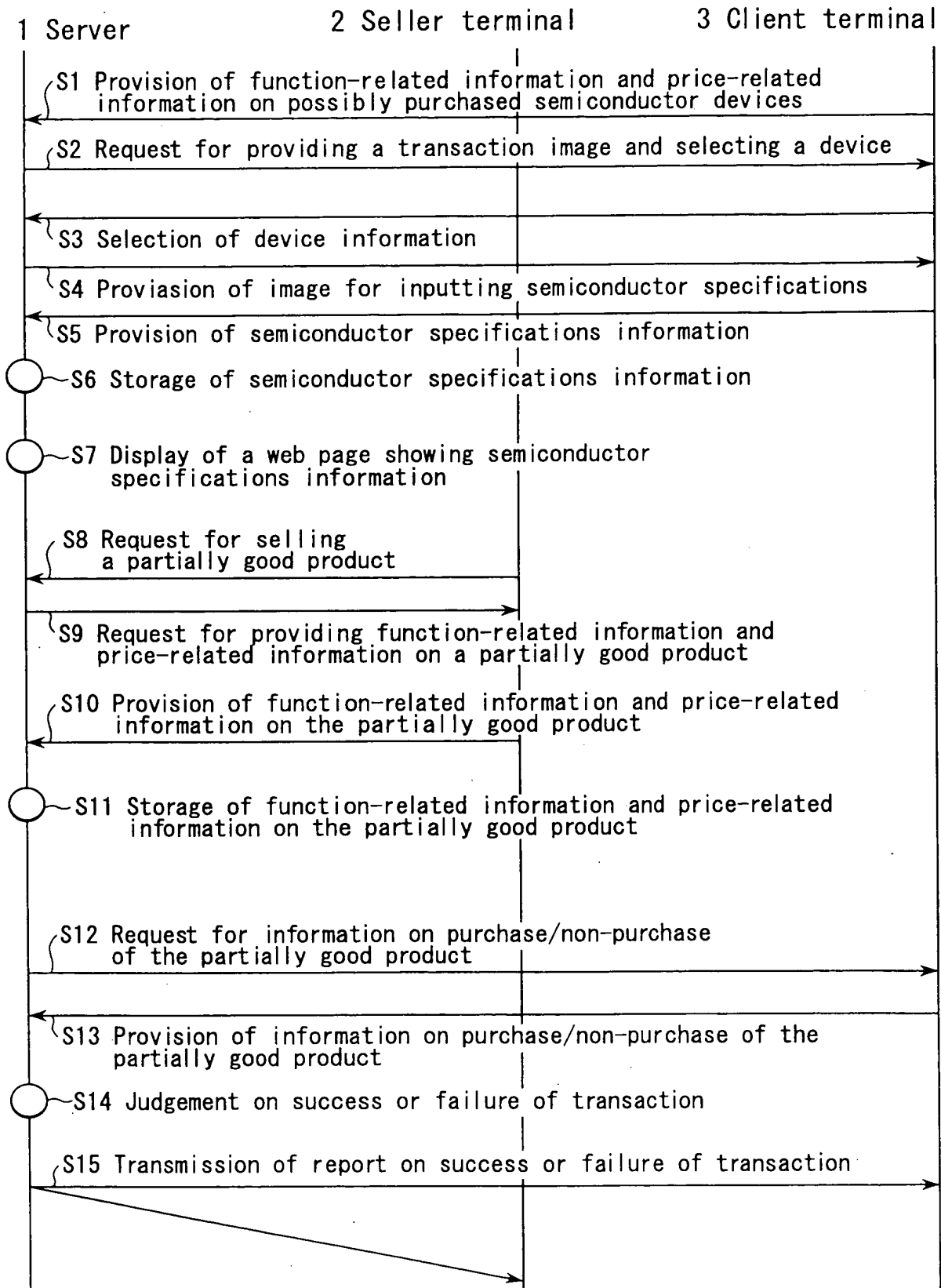


FIG. 7

0964759-092804
T00260"65249660

Check the device you want to buy.

() DRAM
() SRAM
() FLASH

OK 71 Cancel 72

FIG. 8

① Degree of integration () M
② Access time () nsec
③ Operation mode ()
④ Desired price ()
⑤ Desired date of delivery ()

OK 71 Cancel 72

FIG. 9

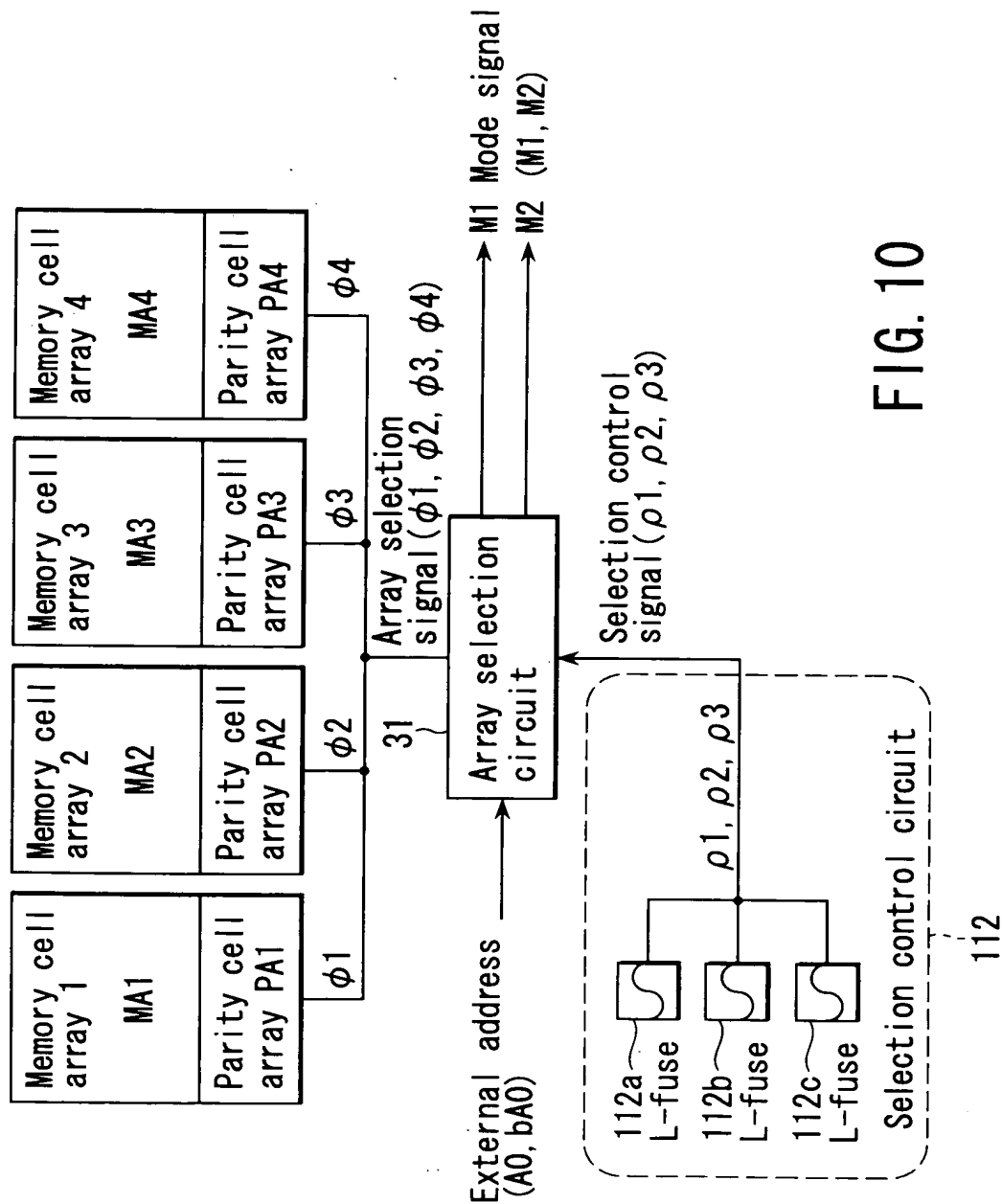


FIG. 10

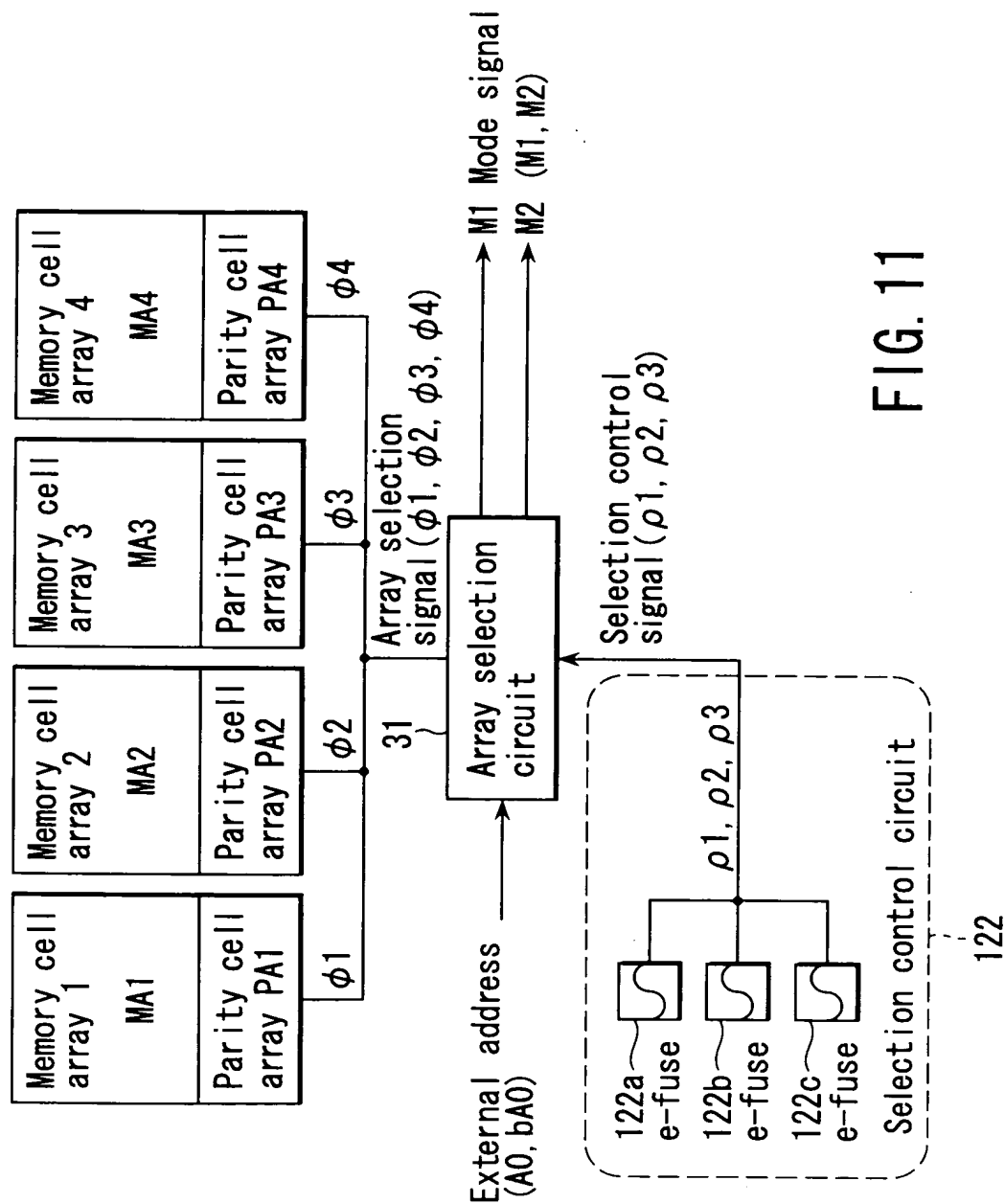


FIG. 11

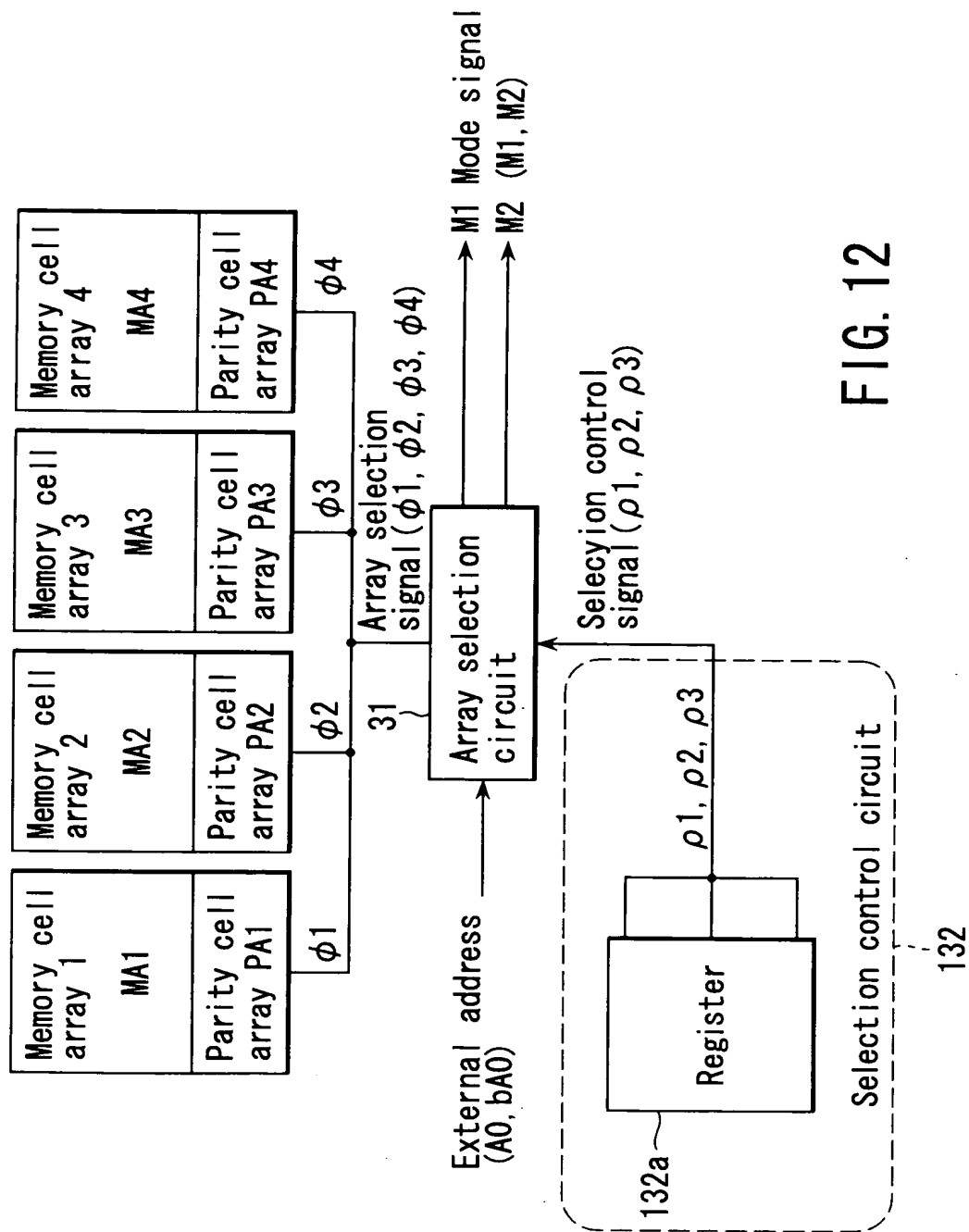


FIG. 12

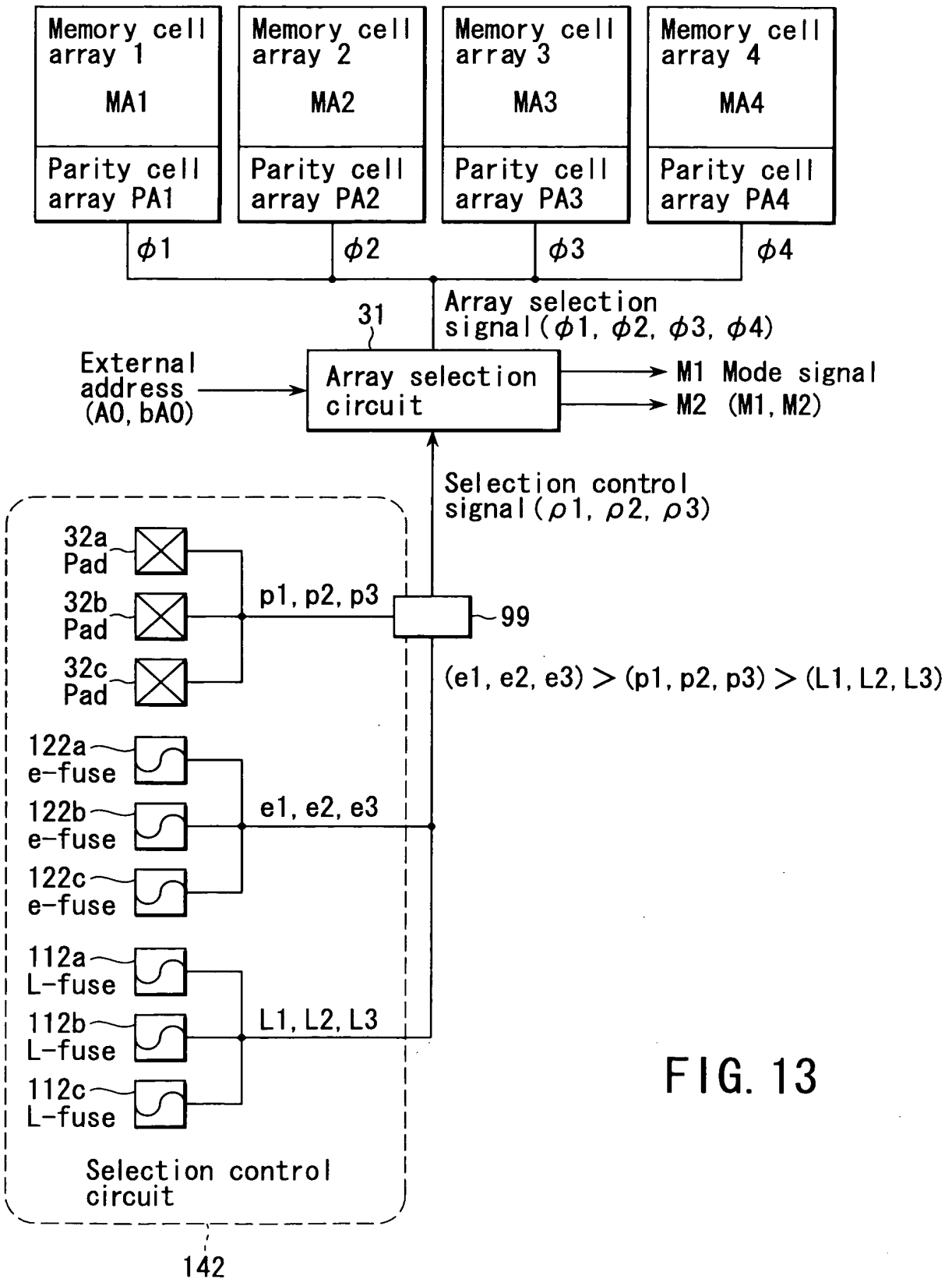


FIG. 13